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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/529,175	03/23/2005	Hidetada Tokioka	403357/FUKAMI	4211

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EXAMINER	
CHOWDHURY, AFROZA Y	
ART UNIT	**PAPER NUMBER**
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/529,175	TOKIOKA ET AL.	
	Examiner	Art Unit	
	Afroza Y. Chowdhury	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 June 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 11-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 11-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/23/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 9 and 10 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Species II, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on June 25, 2007.

2. Applicant's election without traverse of Species I in the reply filed on June 25, 2007 is acknowledged.

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-7 and 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kasai (US Pub. 2003/0030602) in view of Fruehauf (US Pub. 2004/0100430).

As to claim 1, Kasai discloses a current supply circuit providing an output current corresponding to digital data of n bits (wherein n is an integer not less than 2), comprising:

a current driving device (fig. 4(214), driving transistor, page 3, [0067]);

a current output node (fig. 4, page 3, [0064]) electrically connected to a first power supply node (fig. 4, page 3, [0064], Vdd) via said current driving device during current supply;

a current control circuit (fig. 1, 4(210), page 4, [0074] - 0075]) provided between a second power supply node (fig. 4, page 3, [0065], ground voltage) and said current output node (fig. 4, page 3, [0064]) and receiving digital data corresponding to the digital data (fig. 4, page 3, [0068]), for controlling current flowing in a current path including said current output node (fig. 4, page 3, [0064]), between the first power supply (fig. 4, page 3, [0064], Vdd) and second power supply (fig. 4, page 3, [0065], ground voltage) nodes during the current supply.

Kasai does not explicitly teach a voltage regulating circuit to force a change in voltage on current output node based on the digital data.

Fruehauf teaches a voltage regulating circuit for an active matrix driving circuit.

Therefore, it would have been obvious to one skill in the art at the time of invention was made to incorporate Fruehauf's voltage regulating circuit into Kasai's display device to design a current supply circuit for a display device in order to regulate the voltage on current node based on the digital data.

As to claim 2, Kasai teaches a current supply circuit wherein current driving device includes a field effect transistor (fig. 4(214), driving transistor, page 3, [0067]) having a source and a drain electrically connected to the first power supply node (fig. 4, page 3, [0064], Vdd) and said current output node (fig. 4, page 3, [0064]), respectively,

and a gate, and the gate and drain of said field effect transistor are electrically connected during the current supply.

As to claim 3, Kasai teaches a current supply circuit wherein, during the current supply, the voltage on current output node (fig. 4, page 3, [0064]) settles to a certain voltage corresponding to a level of the output current depending on characteristics of current driving device (fig. 4(214), driving transistor, page 3, [0067]).

Kasai does not teach a voltage regulating circuit and steady state voltage on current output node.

Fruehauf teaches a voltage regulating circuit for an active matrix driving circuit.

Therefore, it would have been obvious to one skill in the art at the time of invention was made to incorporate Fruehauf's voltage regulating circuit into Kasai's display device to design a current supply circuit for a display device in order to regulate the voltage on current output node closer to the steady voltage depending on the digital data.

As to claim 4, Kasai discloses a precharge circuit (fig. 18, page 8, [0118]) precharging, prior to supply of the output current, current output node to a predetermined voltage;

Kasai does not teach a current supply circuit with a voltage regulating circuit.

Fruehauf teaches a voltage regulating circuit for an active matrix driving circuit.

Therefore, it would have been obvious to one skill in the art at the time of invention was made to incorporate Fruehauf's voltage regulating circuit into Kasai's display device to design a current supply circuit for a display device where a precharge regulating circuit exchanging electric charge corresponding to the digital data with current output node.

As to claim 5, Kasai teaches a current supply circuit wherein said precharge regulating circuit (fig. 18, page 8, [0118]) includes n regulating units corresponding to the respective n bits of the digital data, and said n regulating units include:

n respective capacitors (fig. 1, 4(230), page 3, [0064]) charged by respective first to n-th voltages prior to the supply of the output current;

and n respective switching devices (fig. 1, 6(41), page 4, [0076]) provided between said n respective capacitors and said current output node, and each of said n switches turns on or off depending on one corresponding bit of the digital data during the current supply.

As to claim 6, Kasai discloses a current supply circuit wherein, during the current supply, the voltage on said current output node settles to a constant voltage (page 8, [0118], Vp) corresponding to a level of the output current depending on characteristics of said current driving device,

and the predetermined voltage (page 8, [0118]) the first to n-th voltages (fig. 18), and capacitances of said n capacitors (fig. 1, 4(230), page 3, [0064]) are designed, for

each of at least one of the combinations of the n bits of the digital data, based on conservation of charge that reflects the constant voltage between before and after at least one of said n switching devices (fig. 1, 6(41), page 4, [0076]), corresponding to the n bits, is turned on.

As to claim 7, Kasai teaches a current supply circuit wherein said current control circuit includes n constant-current supplies (fig. 1, 4, page 4, [0071]) corresponding to the respective n bits of the digital data and connected in parallel to said current output node,

and said n constant-current supplies (fig. 1, 4, page 4, [0071]) generate, corresponding to the n respective bits (fig. 1), first to n-th currents between the second power supply node and said current output node.

As to claim 11, A display device producing a gray-scale display corresponding to image data of n bits (wherein n is an integer not less than 2), comprising:

a current supply circuit (fig. 1, 4(210), page 4, [0074] - 0075]) for supplying a display current corresponding to the image data;

a plurality of pixel circuits (fig. 1, 4, page 3, [0059]), each pixel circuit (fig.4) including a current-driven light-emitting device (fig. Fig. 4(220), page 3, [0061]) providing a brightness corresponding to a supplied current and a pixel driving circuit for supplying said current-driven light-emitting device (fig. Fig. 4(220), page 3, [0061]) with a current corresponding to the display current;

and a current data line (fig. 1, [0061]) for conveying the display current, which is provided by said current supply circuit, to said plurality of pixel circuits (fig. 1, 4, page 3, [0059]),

wherein said pixel driving circuit has a current driving device (fig. 4(214), driving transistor, page 3, [0067]) connected between said current data line and a first power supply node (fig. 4, page 3, [0064], Vdd) during a predetermined period (page 3, [0061]) in which the display current is conveyed thereto, and supplies said current-driven light-emitting device (fig. Fig. 4(220), page 3, [0061]) with a current corresponding to the display current conveyed during the predetermined period (page 3, [0061]),

a current control circuit (fig. 1, 4(210), page 4, [0074] - 0075]) provided between a second power supply node (fig. 4, page 3, [0065], ground voltage) and said current output node (fig. 4, page 3, [0064]) and receiving digital data corresponding to the digital data (fig. 4, page 3, [0068]), for controlling current flowing in a current path including said current output node (fig. 4, page 3, [0064]), between the first power supply (fig. 4, page 3, [0064], Vdd) and second power supply (fig. 4, page 3, [0065], ground voltage) nodes during the current supply.

Kasai does not explicitly teach a voltage regulating circuit to force a change in voltage on current output node based on the digital data.

Fruehauf teaches a voltage regulating circuit for an active matrix driving circuit.

Therefore, it would have been obvious to one skill in the art at the time of invention was made to incorporate Fruehauf's voltage regulating circuit into Kasai's display device to design a current supply circuit for a display device in order to regulate

the voltage on current node based on the digital data.

As to claim 12, Kasai teaches a display device wherein current control circuit (fig. 1, 4(210), page 4, [0074] - 0075], [0077]) includes n constant-current supplies (fig. 18, [0071], [0077]) corresponding to the n respective bits of the image data and connected in parallel to current data line,

and said n constant-current supplies (fig. 18, [0071], [0077]) generate first to n-th currents on said current data line based on the n respective bits.

As to claim 13, Kasai teaches a current supply circuit wherein, during the current supply, the voltage on current output node (fig. 4, page 3, [0064]) settles to a certain voltage corresponding to a level of the output current depending on characteristics of current driving device (fig. 4(214), driving transistor, page 3, [0067]).

Kasai also discloses a precharge circuit (fig. 18, [0118]) precharging, prior to supply of the output current, current output node to a predetermined voltage.

Kasai does not explicitly teach a current supply circuit including a voltage regulating circuit and steady state voltage on current output node.

Fruehauf teaches a voltage regulating circuit for an active matrix driving circuit.

Therefore, it would have been obvious to one skill in the art at the time of invention was made to incorporate Fruehauf's voltage regulating circuit into Kasai's display device to design a current supply circuit for a display device in order to regulate the voltage on current output node closer to the steady voltage depending on the digital

data.

Claim 14 is rejected the same as claim 5.

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kasai (US Pub. 2003/0030602) in view of Fruehauf (US Pub. 2004/0100430) and in further view of Koyama et al. (US Pub. 2002/0024054).

As to claim 8, Kasai (as modified by Fruehauf) teaches a current supply circuit.

Kasai (as modified by Fruehauf) does not explicitly teach that the first n-th currents are set in gradations in a power of 2 corresponding to a predetermined weighting of the n bits of the digital data.

Koyama et al. teaches an n-bit display device where a display period divided into n periods, and the length ration of each period is set to powers of 2 (page 5, [0066]).

Therefore, it would have been obvious to one skill in the art at the time of invention was made to combine the electronic device of Koyama et al. with the current supply circuit of Kasai (as modified by Fruehauf) to make a current supply circuit with gradations with power of two.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Afroza Y. Chowdhury whose telephone number is 571-270-1543. The examiner can normally be reached on 7:30-5:00 EST, 5/4/9.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amare Mengistu can be reached on 571-272-7674. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

AC

7/3/2007

AMARE MENGISTU
SUPERVISORY PATENT EXAMINER